Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS**

1. **A**
2. **B**
3. **J**
4. **K**
5. **C**
6. **D**
7. **VSS**
8. **E**
9. **F**
10. **L**
11. **M**
12. **G**
13. **H**
14. **VDD**

**.073”**

**.071”**

**12 11 10**

**13**

**14**

**1**

**2 3 4 5**

**9**

**8**

**7**

**6**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VDD**

**Mask No: 6950**

**APPROVED BY: DK DIE SIZE .071” X .073” DATE: 8/25/21**

**MFG: RCA-HARRIS THICKNESS .020” P/N: CD4070B**

**DG 10.1.2**

#### Rev B, 7/1